Universität Stuttgart

Institut für Nano- und Mikroelektronische Systeme

Master Thesis

Design of a low power hybrid capacitance-to-digital converter on ultra-thin silicon chips

Arbeitsbereich:
ASICs

Ausrichtung:

☒Entwicklung & Simulation
☒Layout
☐Charakterisierung
☐Programmierung
☒Hardware-Entwicklung
☐Messtechnik
☐Machbarkeitsstudie

Studiengang:

☒Elektro- und Informationstechnik
☐Physik
☐Biologie
☐Informatik
☐Maschinenbau

Einstieg:
01.04.2018

Umfang:
6 Monate

Vorkenntnisse:

☒digitale Schaltungstechn.
☒analoge Schaltungstechn.
☒SPICE Simulation
☒Layout-Erfahrung
☐Programmierkenntnisse
☐elektr. Messtechnik

Ansprechpartner:
Mourad Elsobky

Tel: 0711 21855-329

E-Mail:
elsobky@ims-chips.de

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Motivation

Many industrial institutions adapted the concept of Internet of things and its industrial framework “Industrie 4.0”. An easy to use smart badge with ultra-thin form factor is expected to help companies to mitigate faster to “Industrie 4.0” by attaching the badge to supply chain components and to their end products. These smart badges could form wireless sensor nodes in an interconnected network. Each node should be able to monitor and store the product’s status and its surrounding environmental conditions as well as reporting any violation to predefined events.

Scope of Work

Using the XFAB 0.18 µm technology, a capacitance-to-digital converter (CDC) should be designed for interfacing with mechanically flexible capacitive sensors. The CDC should cover a wide dynamic range with a resolution of 16 bits. The design should target a low power consumption of less than 10 µW at Nyquist rate of 1 kSa/s.
In the scope of this thesis, the following tasks should be scientifically investigated and documented:

- ✓ Literature review and comparison between the state of the art CDC architectures in terms of power and accuracy.
- ✓ Modeling of the complete CDC system using MATLAB and verilogA
- ✓ Mixed-signal transistor-level design and simulation
- ✓ Layout and a clear chance of taping out
- ✓ Benchmarking of the implemented CDC

References

[1] M. Ghanbari, J. Tsai, A. Nirmalathas, R. Muller, S. Gambini, “An Energy-Efficient Miniaturized Intracranial Pressure Monitoring System”, IEEE JSSC, Mar 2017.
[2] S. Oh, W. lung, K. Yang, D. Blaauw, D. Sylvester, “15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR”, 2014 Symposium on VLSI Circuits Dig. Tech. Papers.
[3] H. Ha, D. Sylvester, D. Blaauw, J. Sim,“A 160nW 63.9fJ/conversion-step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes”, ISSCC Dig. Tech. Papers, Feb. 2014.

Key Words

IoT, Industrie 4.0, Flexible Sensor Systems, Ultra-Thin Chips , Circuit Design, Low Power, Capacitance-to-Digital Converters.