Institut für Mikroelektronik Stuttgart
Stiftung des bürgerlichen Rechts

Status:
2022-07-06

Working Area:
ASIC Design

Topics:
☒Development & Simulation
☐PCB design
☐Characterization
☒Programming
☒Hardware Design
☐Measuring
☐Feasibility study

Study course:
☒Electrical Engineering

Begin:
2022-08-15

Duration:
6 Months

Proficiency:
☒digital circuit design
☒analog circuit design
☒SPICE Simulation
☐Layout knowledge
☐programming skills
☐electrical measurements

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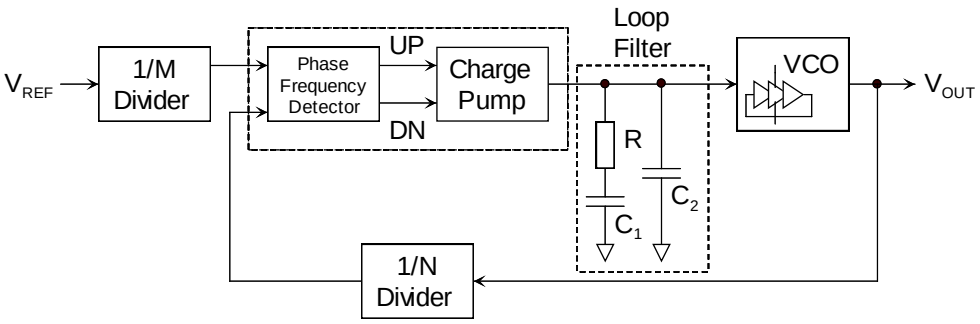
Master Thesis

Design of an integrated phase-locked-loop circuit in 0.18 µm CMOS technology for quantum sensors

Motivation

Quantum sensors are a possible future technology, which are currently transferred from physical research into today's markets. High sensitivity is thereby one of the great advantages of quantum sensors. With this also a high precision signal processing is needed, where phase-locked-loop (PLL) circuits play an important role. A PLL is an advanced circuit which can be used to generate or synchronize high frequency periodic signals. Together with a lock detector, this PLL is to be used for ODMR measurements on quantum pressure sensors.



Description

Within your thesis a PLL shall be analyzed, simulated and transferred into a concrete layout. Therefore a 0.18 µm CMOS technology is used.
A general setup of a PLL can be seen in the block diagram above. It's a complex, non-linear loopback circuit.
The detailed possible tasks are summarized below:

- ✓ Literature study on PLL circuits with lock detectors for quantum sensors and ODMR measurement
- ✓ Conceptual design of the PLL
- ✓ Development and simulation of the single units of the PLL with Cadence Tools (schematic and layout)
- ✓ Establishing of a test environment to evaluate the design
- ✓ Thesis writing and final presentation

Prerequisites

- ✓ Basic knowledge on mixed signal design is preferable