

Status:
2022-07-06

Working Area:
ASIC Design

- Topics:**
- Development & Simulation
 - PCB design
 - Characterization
 - Programming
 - Hardware Design
 - Measuring
 - Feasibility study

Study course:
 Electrical Engineering

Begin:
2022-08-15

Duration:
6 Months

- Proficiency:**
- digital circuit design
 - analog circuit design
 - SPICE Simulation
 - Layout knowledge
 - programming skills
 - electrical measurements

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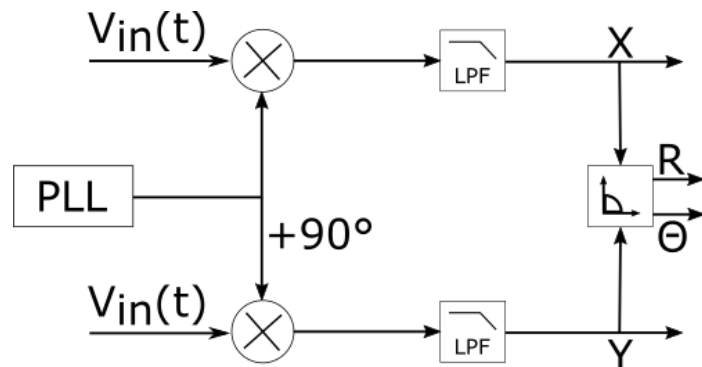
Master Thesis

Design of an integrated Lock-Detection circuit in 0.18 μm CMOS technology for quantum sensors

Motivation

Quantum sensors are a possible future technology, which are currently transferred from physical research into today's markets. High sensitivity is thereby one of the great advantages of quantum sensors. With this also a high precision signal processing is needed, where lock detectors play an important role.

With lock detectors it's possible to measure small signals in very noisy environments and that's why they are beneficial for the advanced signal processing of quantum sensors. Together with a phase-locked-loop (PLL), this lock detector is to be used for ODMR measurements on quantum pressure sensors.



Description

A PLL needed as an input for the lock detector can be either used from an existing circuit or from a simulation model. The focus of this master thesis is on the Lock-Detector, which shall be analyzed, simulated and transferred into a concrete layout in a 0.18 μm CMOS technology. A general setup of a lock detector can be seen in the block diagram above.

The detailed tasks are summarized below:

- ✓ Literature study on Lock Detectors with PLL circuits for quantum sensors and ODMR measurement
- ✓ Conceptual design of a lock-detection circuit.
- ✓ Design and Simulation of the Lock-Detector with Cadence-Tools (schematic and layout)
- ✓ Establishing of a test environment to evaluate the design
- ✓ Thesis writing and final presentation

Prerequisites

- ✓ Basic knowledge on mixed signal design is preferable